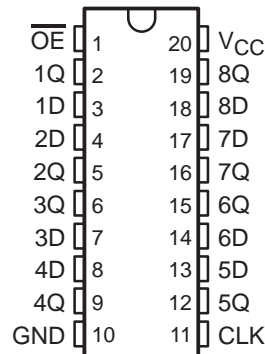


# CD74FCT374 BiCMOS OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCBS739 – JULY 2000

- BiCMOS Technology With Low Quiescent Power
- 3-State Outputs Drive Bus Lines Directly
- Buffered Inputs
- Noninverted Outputs
- Input/Output Isolation From  $V_{CC}$
- Controlled Output Edge Rates
- 48-mA Output Sink Current
- Output Voltage Swing Limited to 3.7 V
- SCR Latch-Up-Resistant BiCMOS Process and Circuit Design
- Package Options Include Plastic Small-Outline (M) and Shrink Small-Outline (SM) Packages and Standard Plastic (E) DIP

E, M, OR SM PACKAGE  
(TOP VIEW)



## description

The CD74FCT374 is an octal, edge-triggered, D-type flip-flop that uses a small-geometry BiCMOS technology and features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. This device is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The output stage is a combination of bipolar and CMOS transistors that limits the output high level to two diode drops below  $V_{CC}$ . This resultant lowering of output swing (0 V to 3.7 V) reduces power-bus ringing [a source of electromagnetic interference (EMI)] and minimizes  $V_{CC}$  bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 mA.

The eight flip-flops enter data into their registers on the low-to-high transition of the clock (CLK). The output-enable ( $\overline{OE}$ ) input controls the 3-state outputs and is independent of the register operation. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

A buffered  $\overline{OE}$  input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The CD74FCT374 is characterized for operation from 0°C to 70°C.



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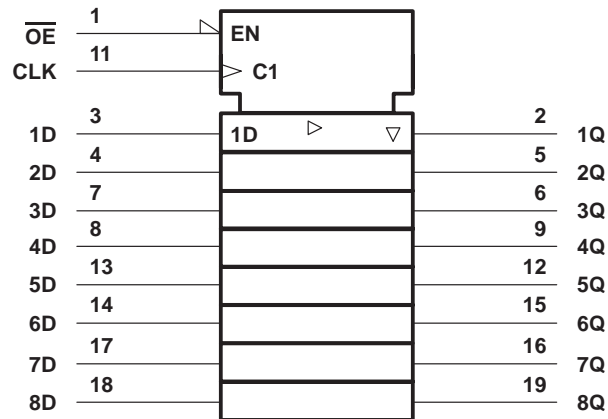
# CD74FCT374 BiCMOS OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCBS739 – JULY 2000

FUNCTION TABLE  
(each flip-flop)

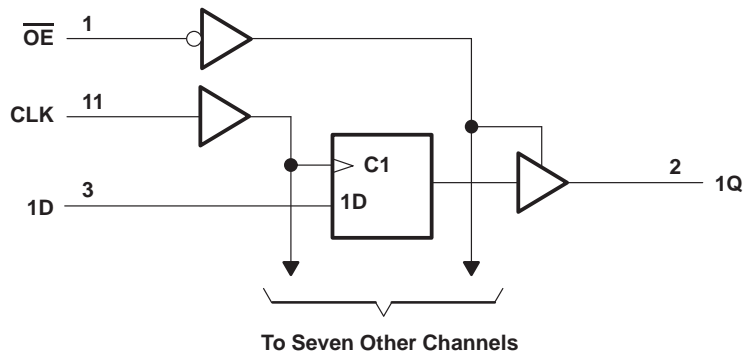
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



# CD74FCT374

## BiCMOS OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCBS739 – JULY 2000

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

DC supply voltage range, $V_{CC}$	–0.5 V to 6 V
DC input clamp current, $I_{IK}$ ( $V_I < -0.5$ V)	–20 mA
DC output clamp current, $I_{OK}$ ( $V_O < -0.5$ V)	–50 mA
DC output sink current per output pin, $I_{OL}$	70 mA
DC output source current per output pin, $I_{OH}$	–30 mA
Continuous current through $V_{CC}$ , $I_{CC}$	140 mA
Continuous current through GND	400 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): E package	69°C/W
M package	58°C/W
SM package	70°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.75	5.25	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–15	mA
$I_{OL}$	Low-level output current		48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
$T_A$	Operating free-air temperature	0	70	°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
$V_{IK}$	$I_I = -18$ mA	4.75 V		–1.2		–1.2	V
$V_{OH}$	$I_{OH} = -15$ mA	4.75 V	2.4		2.4		V
$V_{OL}$	$I_{OL} = 48$ mA	4.75 V		0.55		0.55	V
$I_I$	$V_I = V_{CC}$ or GND	5.25 V		$\pm 0.1$		$\pm 1$	$\mu\text{A}$
$I_{OZ}$	$V_O = V_{CC}$ or GND	5.25 V		$\pm 0.5$		$\pm 10$	$\mu\text{A}$
$I_{OS}^\ddagger$	$V_I = V_{CC}$ or GND, $V_O = 0$	5.25 V		–60		–60	mA
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.25 V		8		80	$\mu\text{A}$
$\Delta I_{CC}^\S$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.25 V		1.6		1.6	mA
$C_i$	$V_I = V_{CC}$ or GND			10		10	pF
$C_o$	$V_O = V_{CC}$ or GND			15		15	pF

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 100 ms.

§ This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ .



**CD74FCT374**  
**BiCMOS OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP**  
**WITH 3-STATE OUTPUTS**

SCBS739 – JULY 2000

timing requirements over recommended operating conditions, (unless otherwise noted) (see Figure 1)

			MIN	MAX	UNIT
$f_{\text{clock}}$	Clock frequency			70	MHz
$t_w$	Pulse duration	CLK high or low	7		ns
$t_{\text{su}}$	Setup time	Data before CLK↑	2		ns
$t_h$	Hold time	Data after CLK↑	2		ns

switching characteristics over recommended operating conditions,  $V_{\text{CC}} = 5 \text{ V} \pm 0.25 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$	MIN	MAX	UNIT
			TYP			
$f_{\text{max}}$				70		MHz
$t_{\text{pd}}$	CLK	Q	6.6	2	10	ns
$t_{\text{en}}$	$\overline{\text{OE}}$	Q	9	1.5	12.5	ns
$t_{\text{dis}}$	$\overline{\text{OE}}$	Q	6	1.5	8	ns

noise characteristics,  $V_{\text{CC}} = 5 \text{ V}$ ,  $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$

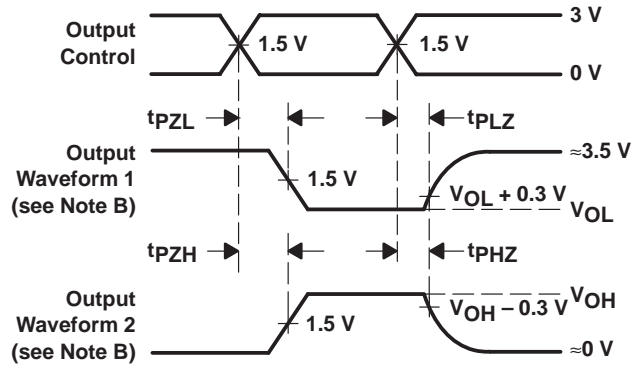
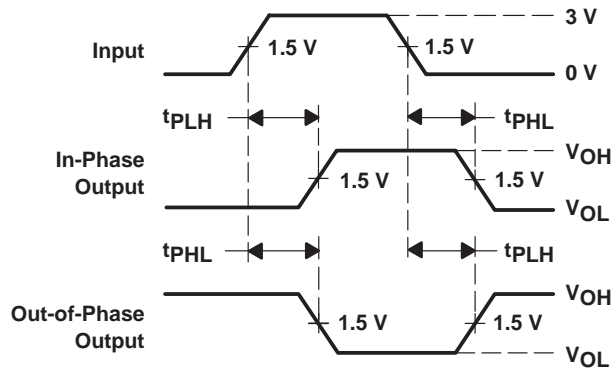
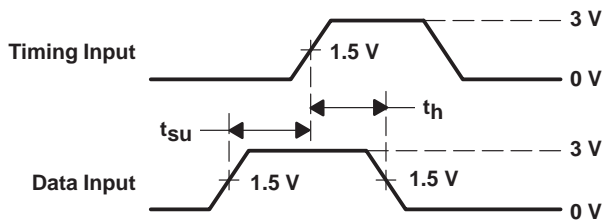
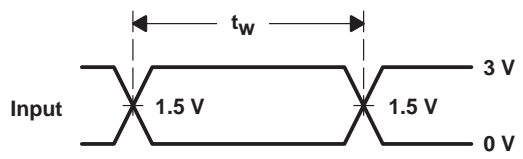
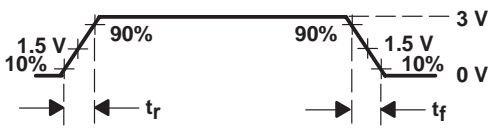
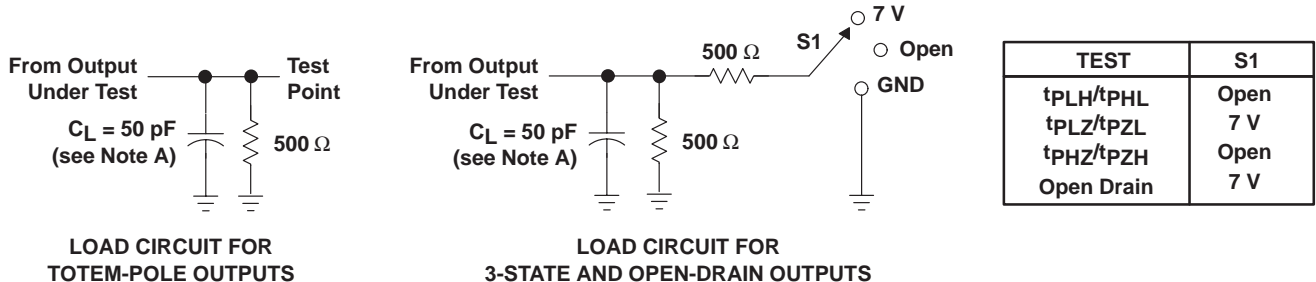
PARAMETER		MIN	TYP	MAX	UNIT
$V_{\text{OL(P)}}$	Quiet output, maximum dynamic $V_{\text{OL}}$		1		V
$V_{\text{OH(V)}}$	Quiet output, minimum dynamic $V_{\text{OH}}$		0.5		V
$V_{\text{IH(D)}}$	High-level dynamic input voltage	2			V
$V_{\text{IL(D)}}$	Low-level dynamic input voltage			0.8	V

operating characteristics,  $V_{\text{CC}} = 5 \text{ V}$ ,  $T_A = 25^\circ$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance	No load, $f = 1 \text{ MHz}$	33	pF



**PARAMETER MEASUREMENT INFORMATION**



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r$  and  $t_f = 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - G. t<sub>PHL</sub> and t<sub>PLH</sub> are the same as t<sub>pd</sub>.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD74FCT374E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74FCT374EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74FCT374M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74FCT374M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74FCT374M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74FCT374M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74FCT374ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74FCT374MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74FCT374SM	OBSOLETE	SSOP	DB	20		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74FCT374M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74FCT374M96	SOIC	DW	20	2000	346.0	346.0	41.0



DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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